Experiment No. 04

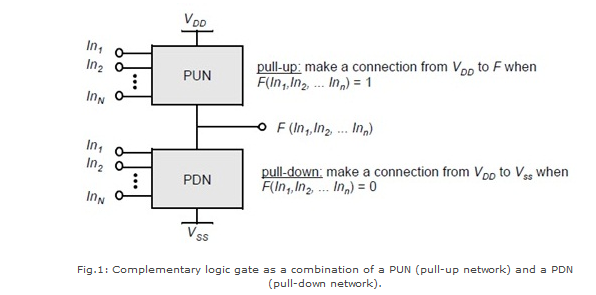
**Schematic of 2-input NAND Gate**

**OBJECTIVE:** To simulate the schematic of the 2-input NAND Gate

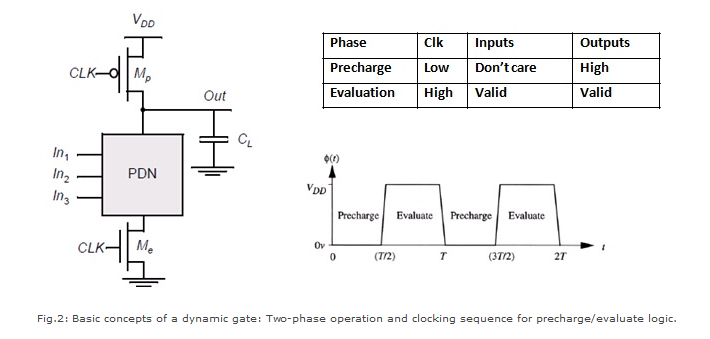
**SOFTWARE**: Electric VLSI , LT Spice

**THEORY:**

**Static logic** is a design methodology in integrated circuit design where there is at all times some mechanism to drive the output either high or low. For example, in many of the popular logic families, such as TTL and traditional CMOS, there is always a low-impedance path between the output and either the supply voltage or the ground. The most widely used logic style is static CMOS. A static CMOS gate is a combination of two networks, called the pull-up network (PUN) and the pull-down network (PDN). The function of the PUN is to provide a connection between the output and VDD anytime the output of the logic gate is meant to be 1 (based on the inputs). Similarly, the function of the PDN is to connect the output to VSS when the output of the logic gate is meant to be 0 (based on the inputs). The PUN and PDN networks are constructed in a mutually exclusive fashion such that, one and only one of these networks is conducting in the steady state.



**Dynamic logic** is a design methodology in integrated circuit design in that it uses a clock signal in its implementation of combinational logic circuits. In dynamic logic, there is not always a mechanism driving the output high or low. In the most common version of this concept, the output is driven high or low during distinct parts of the clock cycle. Dynamic logic requires a minimum clock rate fast enough that the output state of each dynamic gate is used before it leaks out of the capacitance holding that state. The basic construction of a dynamic logic gate is shown in fig.2. The PDN (pull-down network) is constructed exactly as in complementary CMOS. The operation of this circuit is divided into two major phases: precharge and evaluation, with the mode of operation determined by the clock signal CLK.

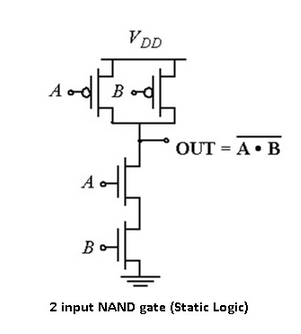


Precharge: When CLK = 0, the output node Out is precharged to VDD by the PMOS transistor Mp. During that time, the evaluate NMOS transistor Me is off, so that the pull-down path is disabled. The evaluation FET eliminates any static power that would be consumed during the precharge period (this is, static current would flow between the supplies if both the pulldown and the precharge device were turned on simultaneously).

Evaluation: For CLK = 1, the precharge transistor Mp is off, and the evaluation transistor Me is turned on. The output is conditionally discharged based on the input values and the pull-down topology. If the inputs are such that the PDN conducts, then a low resistance path exists between Out and GND and the output is discharged to GND. If the PDN is turned off, the precharged value remains stored on the output capacitance CL, which is a combination of junction capacitances, the wiring capacitance, and the input capacitance of the fan-out gates. During the evaluation phase, the only possible path between the output node and a supply rail is to GND. Consequently, once Out is discharged, it cannot be charged again till then next precharge operation. The inputs to the gate can therefore make at most one transition during evaluation.

## Static Logic Design of NAND

The below figure shows a 2-input Complementary MOS NAND gate. It consists of two series NMOS transistors between output and Ground and two parallel PMOS transistors between output and VDD.



If either input A or B is logic 0, at least one of the NMOS transistors will be OFF, breaking the path from output to Ground. But at least one of the PMOS transistors will be ON, creating a path from Output to VDD.

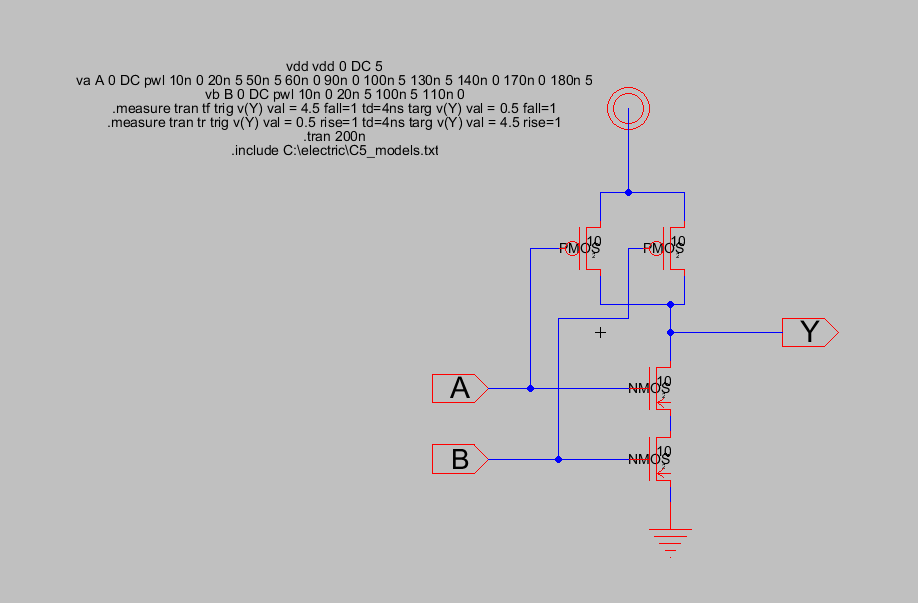
Hence, the output will be high. If both inputs are high, both of the NMOS transistors will be ON and both of the PMOS transistors will be OFF. Hence, the output will be logic low. The truth table of the NAND logic gate given in the below table.

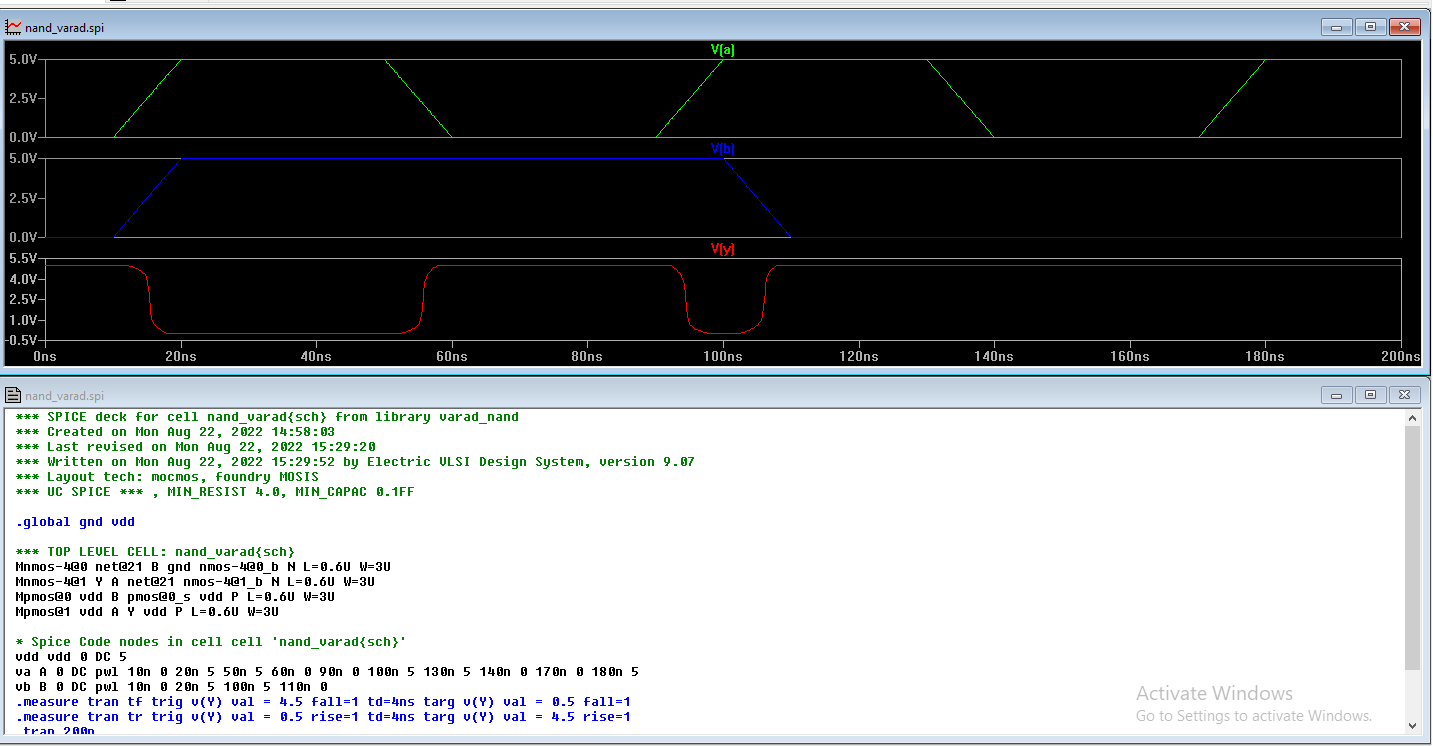
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **A** | **B** | **Pull-Down Network** | **Pull-up**  **Network** | **Y** |
| 0 | 0 | OFF | ON | 1 |
| 0 | 1 | OFF | ON | 1 |
| 1 | 0 | OFF | ON | 1 |
| 1 | 1 | ON | OFF | 0 |

**PROCEDURE:**

1. Open Electric VLSI.
2. In **Files** Menu---click on **new** **library**---Give name to library.
3. In **Edit** Menu---click on **New Cell**---give name to cell---Select view as –schematic.
4. Go to **Components**---Select each required component----do connections.
5. In **Tools** menu---go to **Simulation(spice)**---**Set Spice model**. Select text Spice model and edit it to PMOS or NMOS according to the device.
6. **Create export**s as—A, B (for inputs) and AB (for output)
7. Write Spice code---by clicking on **Misc** in **components** and click on **spice code**.
8. Save library.
9. Simulate the schematic --- in **Tools** menu ----go to **Simulation(spice)**--- click on **Write Spice deck**.
10. LT Spice window gets opened. There Right click on the black window---click on **add trace**.
11. To see fall and rise time--- in **Edit** menu ---click on **SPICE error log**.

**OUTPUT:**





**CONCLUSION:**

Designing and Simulation of the schematic of the 2 input AND Gate using cmos implementation in electric vlsi was performed successfully. The output of cmos was plotted in ltspice and was verified.